Docket No.: 43876-112 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Craig C. HANSEN, et al.	:	Confirmation Number: [conf_no]
Application No.: 09/377,182 Patent No. 6,584,482 B1	:	Group Art Unit: 2124
Filed: August 19, 1999	:	Examiner: David H. Malzahn

For: MULTIPLE ARRAY PROCESSING SYSTEM WITH ENHANCED UTILIZATION AT LOWER PRECISION

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.323

Mail Stop box4
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reviewing the above-identified patent, a minor error, made by applicant, was discovered therein requiring correction in order to conform the Official Record in the application. The error resulted from a draftsman inadvertently replacing the term "Fixed-point" in Figures 5A and 5B as originally filed to "Floating-point" in preparing formal drawings. Figure 5A was printed on the title page of the above patent, and the error was reproduced in the title page as well. A copy of originally filed Figures 5A and 5B are attached hereto as Exhibit A.

It is also clear from the patent specification at column 4 lines 59-61, where figure 5A is described as a group-fixed-point-multiply-and-sum. See also column 5 lines 61-62, where figure 5B is described as a group-fixed-point-multiply-sum-and-add. The record is clear that the term "Floating-point" is an error in Figures 5A and 5B. The error was made in good faith and was of a clerical or typographical nature or of minor character.

The error noted is set forth on the attached copy of form PTO-1050 Rev. 2-93 in the manner required by the Commissioner's Notice.

Specifically, On the Title page of the Letters Patent and on sheet 5 of 13, Figure 5A, sheet 6 of 13, Figure 5B, change "Floating-point" to Fixed-point.

Please charge the $100.00 filing fee to our Deposit Account 500417.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Lawrence T. Cullen
Registration No. 44,489

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Date: January 10, 2005

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,584,482 B1
DATED : June 24, 2003
INVENTOR(S) : Craig C. HANSEN, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page showing the illustrative figure should be deleted to be replaced with the attached title page.

Drawing sheet, consisting of Figs. 5A-5B, should be deleted to be replaced with the drawing sheet, consisting of Figs. 5A-5B, as shown on the attached page.

US006584482B1

(12) **United States Patent**
Hansen et al.

(10) **Patent No.: US 6,584,482 B1**
(45) **Date of Patent: *Jun. 24, 2003**

(54) **MULTIPLIER ARRAY PROCESSING SYSTEM WITH ENHANCED UTILIZATION AT LOWER PRECISION**

(75) Inventors: **Craig C. Hansen**, Los Altos, CA (US); **Henry Massalin**, Sunnyvale, CA (US)

(73) Assignee: **Microunity Systems Engineering, Inc.**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/377,182**

(22) Filed: **Aug. 19, 1999**

Related U.S. Application Data

(63) Continuation of application No. 08/857,596, filed on May 16, 1997, now Pat. No. 5,953,241, which is a continuation-in-part of application No. 08/516,036, filed on Aug. 16, 1995, now Pat. No. 5,742,840.

(60) Provisional application No. 60/021,132, filed on May 17, 1996.

(51) **Int. Cl.**[7] **G06F 17/15**

(52) **U.S. Cl.** **708/523**; 708/420; 708/501; 708/603; 712/221

(58) **Field of Search** 708/523, 501, 708/319, 603, 420; 712/221

(56) **References Cited**

U.S. PATENT DOCUMENTS

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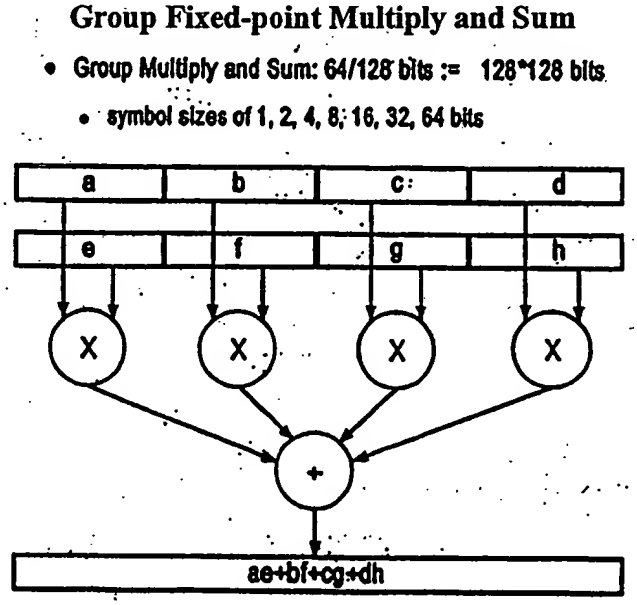
Primary Examiner—David H. Malzahn
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

A multiplier array processing system which improves the utilization of the multiplier and adder array for lower-precision arithmetic is described. New instructions are defined which provide for the deployment of additional multiply and add operations as a result of a single instruction, and for the deployment of greater multiply and add operands as the symbol size is decreased.

23 Claims, 13 Drawing Sheets



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UNITED STATES PATENT AND TRADEMARK OFFICE

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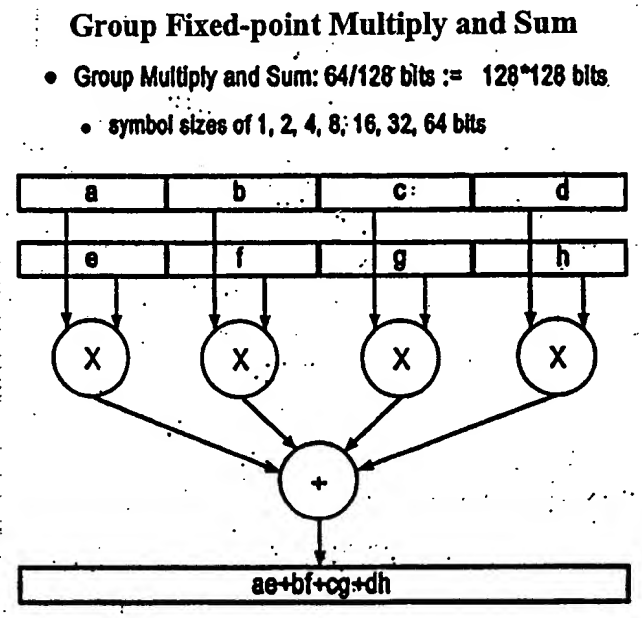
On the Title page of the Letters Patent and on sheet 5 of 13, sheet 6 of 13, change the drawing to the drawing shown below:

Figure 5A



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6,584,482

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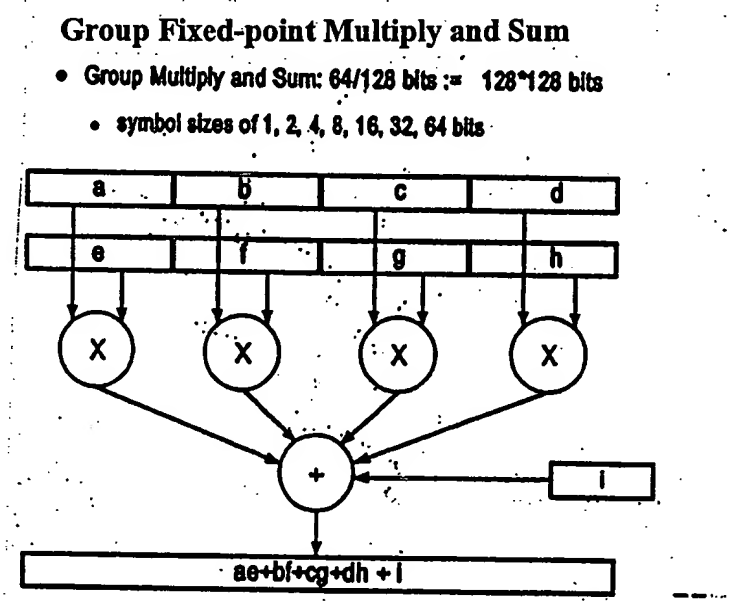
Figure 5B



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